Agilent HCPL-3180 2 Amp Output Current, High Speed IGBT/MOSFET Gate Drive Optocoupler

Data Sheet

Description

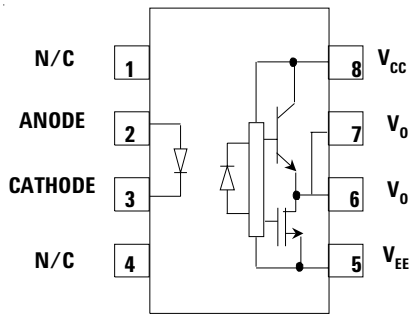
This family of devices consists of a GaAsP LED. The LED is optically coupled to an integrated circuit with a power stage. These optocouplers are ideally suited for high frequency driving of power IGBT and MOSFETs used in Plasma Display Panels, high performance DC/DC convertors and motor control invertor applications.

Ordering Information

Specify part number followed by option number (if desired):

Example : HCPL-3180-XXX

- No option = Standard DIP package, 50 per tube.
- 300 = Gull Wing Surface Mount Option, 50 per tube.
- 500 = Tape and Reel Packaging Option.
- 060 = DIN EN 60747-5-2 Option, VIORM=630 Vpeak (pending approval)



Functional Diagram

Features

- 2 A minimum peak output current
- 250 KHz maximum switching speed
- High speed response: 200 ns max Propagation delay over temperature range
- 10 KV/us minimum common mode rejection (CMR) at V_{CM}=1500 V
- Under voltage lockout protection (UVLO) with hysteresis
- Wide operating temperature range: -40 °C to +100 °C
- Wide V_{CC} operating range: 10 V to 20 V
- 20 ns typ pulse width distortion
- Safety Approvals:
  UL approval pending
  3750 V_{RMS} for 1 minute.
  CSA approval
  DIN EN 60747-5-2 approval pending

Applications

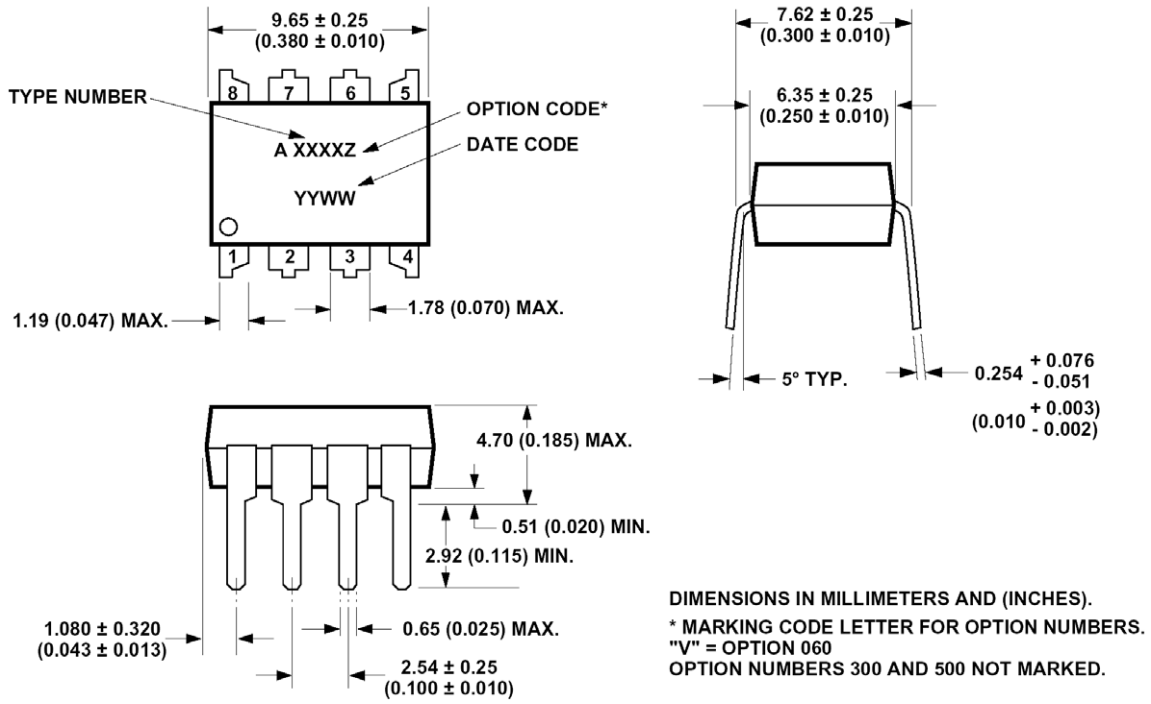
- Plasma Display Panel (PDP)
- Distributed power architecture (DPA)
- Switch mode rectifier (SMR)
- High performance DC/DC convertor
- High performance switch mode power supply (SMPS)
- High performance uninterruptible power supply (UPS)
- Isolated IGBT/Power MOSFET gate drive

A 0.1 uF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Agilent Technologies

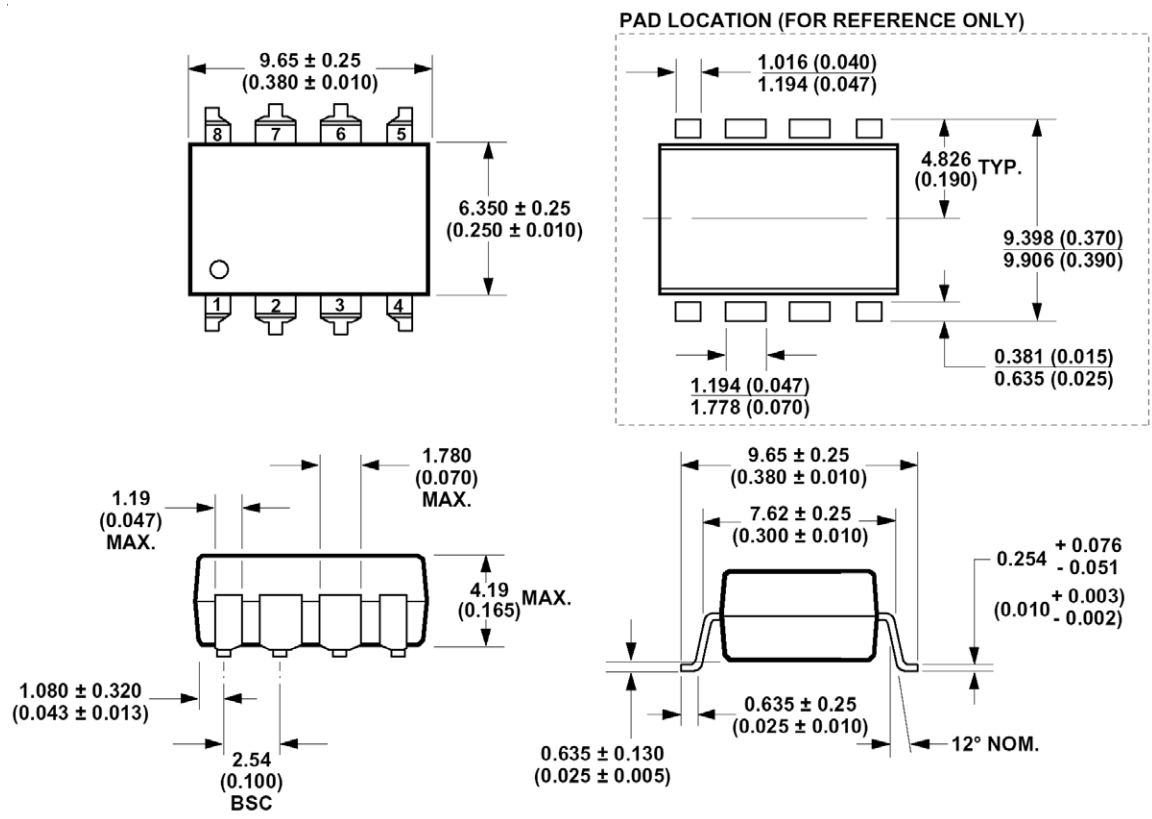
HCPL-3180 Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

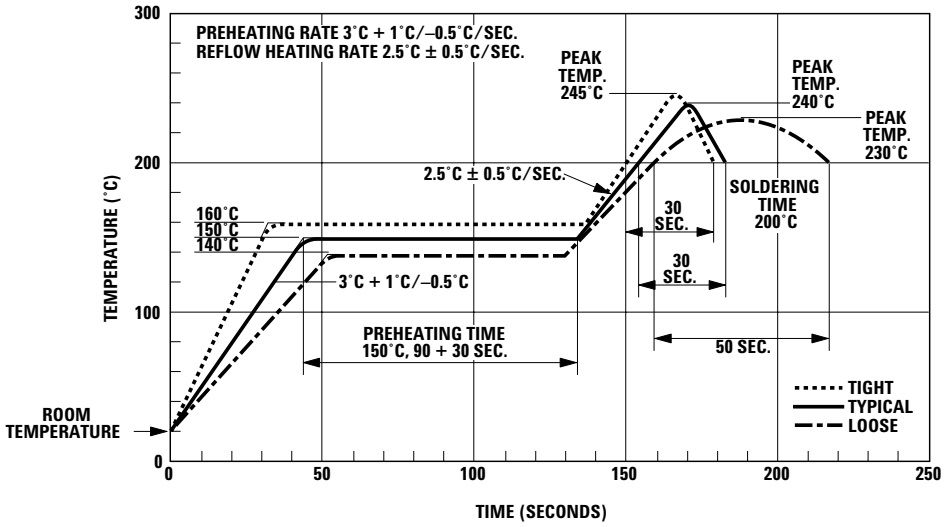
* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

HCPL-3180 Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Solder Reflow Temperature Profile



Regulatory Information
The HCPL-3180 is pending approval by the following organizations:

DIN EN 60747-5-2
Pending approval under DIN EN-60747-5-2 with V_{IORM} = 630 V_{PEAK}

UL
Approval under UL 1577, component recognition program up to V_{ISO} = 2500 V_{RMS}. Pending 3750 V_{RMS}.

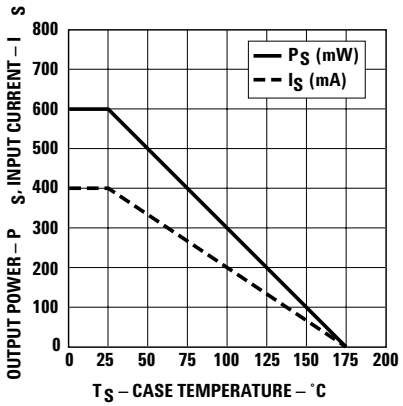
CSA
Approval under CSA Component.

DIN EN 60747-5-2 Insulation Characteristics (HCPL-3180 Option 060)

Description	Symbol	HCPL-3180	Unit
Installation classification per DIN EN 0110 1997-04			
for rated mains voltage 150 Vrms		I - IV	
for rated mains voltage 300 Vrms		I - III	
for rated mains voltage 600 Vrms		I - II	
Climatic Classification		55/100/21	
Pollution Degree (DIN EN 0110 1997 -04)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	Vpeak
Input to Output Test Voltage, Method b* VIORM x 1.875=VPR, 100% Production Test withtm=1 sec, Partial discharge < 5 pC	V_{PR}	1181	Vpeak
Input to Output Test Voltage, Method a* VIORM x 1.5=VPR, Type and Sample Test, tm=60 sec,Partial discharge < 5 pC	V_{PR}	945	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage tini = 10 sec)	V_{IOTM}	6000	Vpeak
Safety-limiting values - maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current**	$I_{S, INPUT}$	230	mA
Output Power**	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at TS, VIO = 500 V	R_S	$>10^9$	W

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (DIN) for a detailed description of Method A and Method B partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	HCPL-3180	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Note
Storage Temperature	T_S	-55	+125	°C	
Junction Temperature	Tj	-40	+125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1s pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	2
Supply Voltage	V_{CC} - V_{EE}	-0.5	25	V	
Output Voltage	$V_{O(PEAK)}$	0	V_{CC}	V	
Output Power Dissipation	P_O		250	mW	3
Total Power Dissipation	P_T		295	mW	4
Lead Solder Temperature	+260 °C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Power Supply	V_{CC} - V_{EE}	10	20	V	
Input Current (ON)	$I_{F(ON)}$	10	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.0	0.8	V	
Operating Temperature	T_A	- 40	100	°C	

Electrical Specifications (DC)
Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig	Note
High Level Output Current	I_{OH}	0.5			A	$V_O = (V_{CC} - 4\ V)$	2, 3	5
		2.0			A	$V_O = (V_{CC} - 10\ V)$	17	2
Low Level Output Current	I_{OL}	0.5			A	$V_O = (V_{EE} + 2.5\ V)$	5, 6	5
		2.0			A	$V_O = (V_{EE} + 10\ V)$	18	2
High Level Output Voltage	V_{OH}	$V_{CC} - 4$			V	$I_O = -100$ mA	1, 3 19	6, 7
Low Level Output Voltage	V_{OL}			0.5	V	$I_O = 100$ mA	4, 6 20	
High Level Supply Current	I_{CCH}		3.0	6.0	mA	Output Open $I_F = 10$ to 16 mA	7, 8	
Low Level Supply Current	I_{CCL}		3.0	6.0	mA	Output Open $VI_F = -3.0$ to 0.8 V	9, 15, 21	
Threshold Input Current Low to High	I_{FLH}			8.0	mA	$I_O = 0$ mA $V_O > 5$ V		
Threshold Input Voltage High to Low	V_{FHL}	0.8			V	I_F - 10 mA	16	
Input Forward Voltage	V_F ∇	1.2	1.5	1.8	V			
Temperature Coefficient of Forward Voltage	$\Delta V_F / T_A$		-1.6		mV/°C			
UVLO Threshold	V_{UVLO+}		7.9		V	$V_O > 5$ V $I_F = 10$ mA	22, 34	
	V_{UVLO-}		7.4		V			
UVLO Hysteresis	$UVLO_{HYST}$		0.5		V			
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ uA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, $V_F = 0$ V		

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig	Note
Propagation Delay Time to High Output Level	t_{PLH}	50	150	200	ns	I_F = 10 mA R_g = 10 Ω f = 250 kHz Duty Cycle = 50% C_g = 10 nF	10, 11, 12, 13, 14, 23	16
Propagation Delay Time to Low Output Level	t_{PHL}	50	150	200	ns			
Pulse Width Distortion	PWD		20	65	ns			12
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-90		90	ms		35, 36	17
Rise Time	t_r		25		ns	C_L = 1 nF R_g = 0 Ω	23	
Fall Time	t_f		25		ns			
UVLO Turn On Delay	$t_{UVLO\ ON}$		2.0		us		22	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.3		us			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	10			kV/µs	T_A = +25 °C I_f = 10 to 16 mA V_{CM} = 1.5 kV V_{CC} = 20 V	24	13, 14
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	10			kV/µs	T_A = +25 °C V_f = 0 V V_{CM} = 1.5 kV V_{CC} = 20 V V_{CM} = 1.5 kV		13, 15

Package Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	2500			V_{rms}	T_A = +25 °C, RH < 50%		8, 9
Input-Output Resistance	R_{I-O}		1011		Ω	V_{I-O} = 500 V		9
Input-Output Capacitance	C_{I-O}		1		pF	Freq = 1 MHz		

Notes:

1. Derate linearly above +70 °C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 us, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See Application section for additional details on limiting I_{OL} peak.
3. Derate linearly above +70 °C, free air temperature at the rate of 4.8 mW/°C.
4. Derate linearly above +70 °C, free air temperature at the rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed +125 °C.
5. Maximum pulse width = 50 us, maximum duty cycle = 0.5%.
6. In this test, V_{OH} is measured with a dc load current. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 3000 V_{rms} for 1 second (leakage detection current limit I_{I-O} < 5 uA).
9. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
10. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal
11. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions
12. PWD is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
13. Pin 1 and 4 need to be connected to LED common.

14. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. $V_O > 10.0$ V).
15. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. $V_O < 1.0$ V).
16. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal
17. The difference between t_{PHL} and t_{PLH} between any two HCPL-3180 parts under same test conditions.

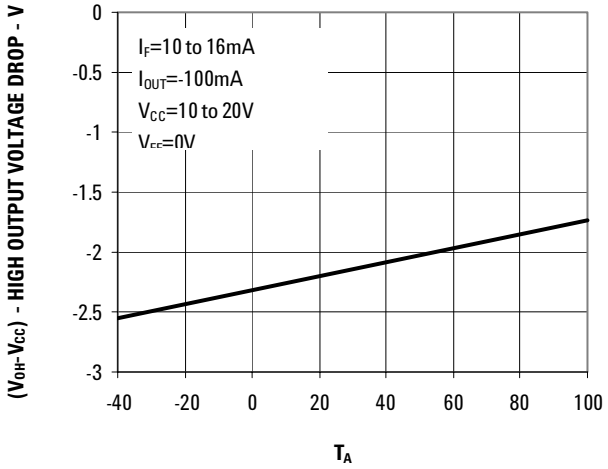


Figure 1. V_{OH} Vs Temperature

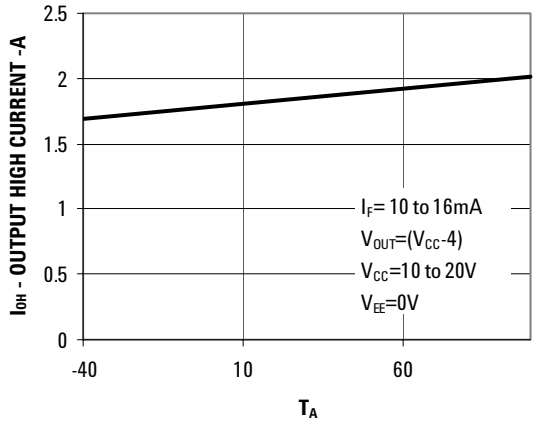


Figure 2. I_{OH} Vs Temperature

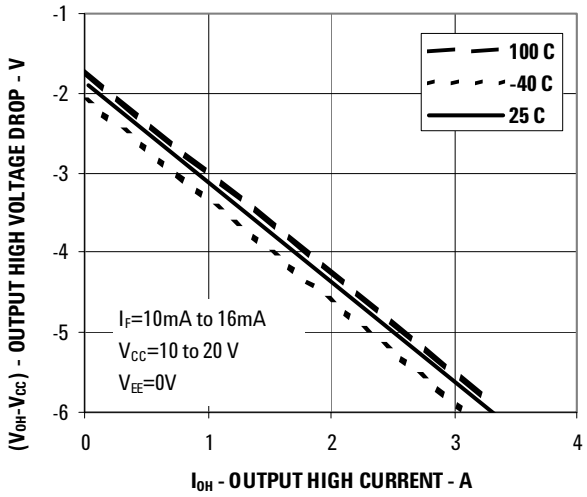


Figure 3. V_{OH} Vs I_{OH}

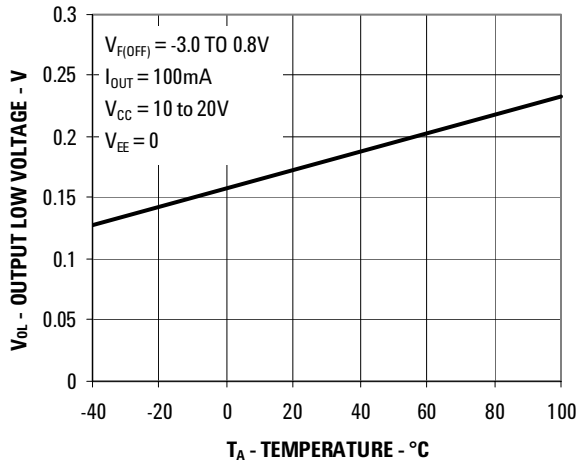


Figure 4. V_{OL} Vs Temperature

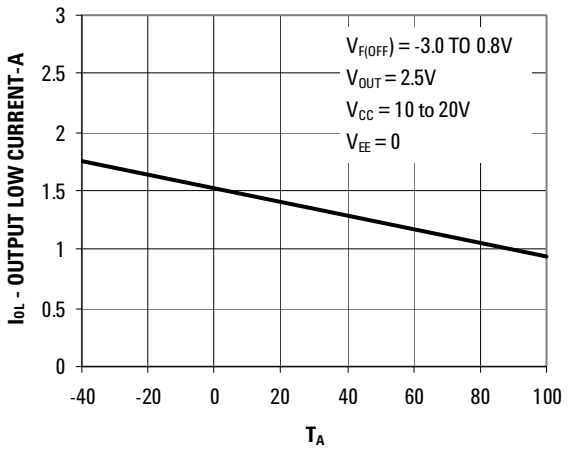


Figure 5. I_{OL} Vs Temperature

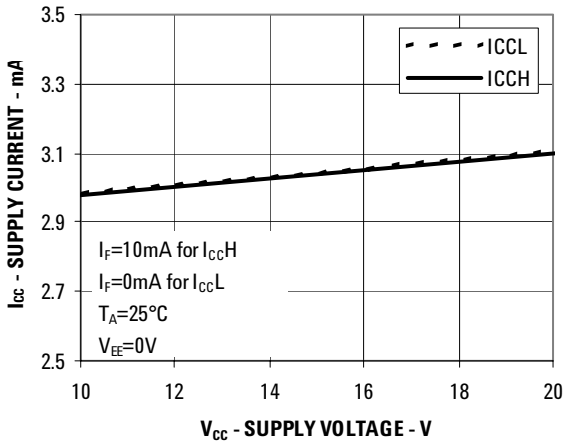


Figure 8. I_{CC} Vs V_{CC}

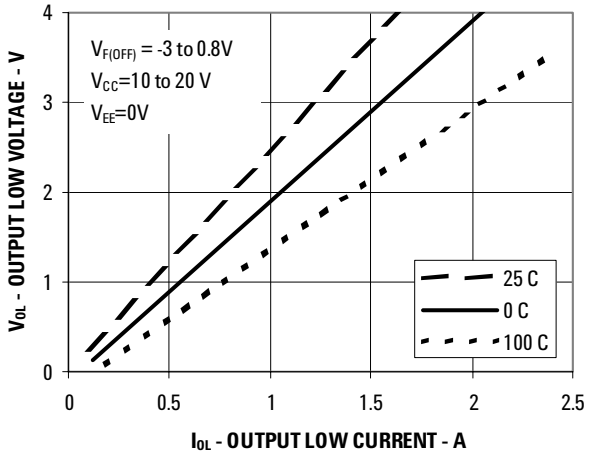


Figure 6. V_{OL} Vs I_{OL}

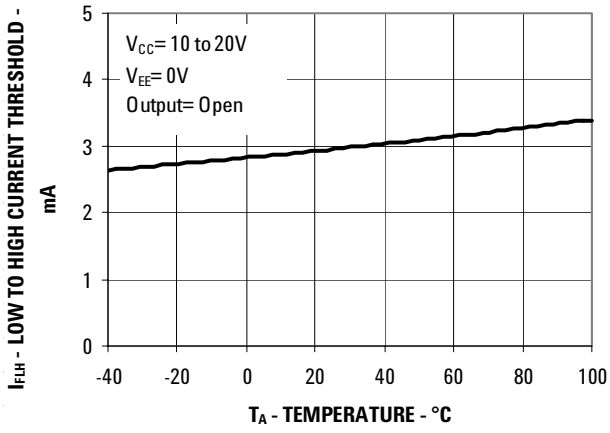


Figure 9. IFLH Vs Temperature

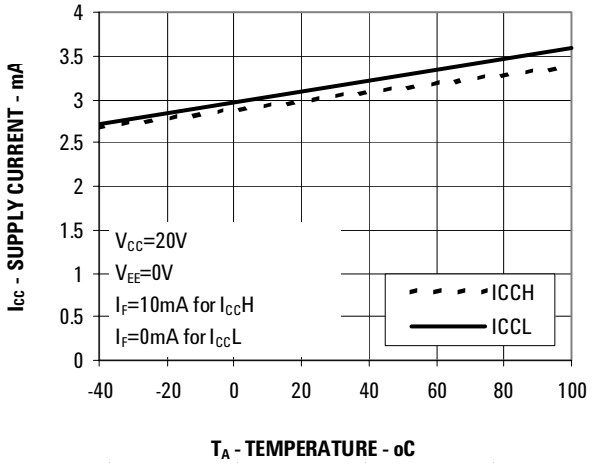


Figure 7. I_{CC} Vs Temperature

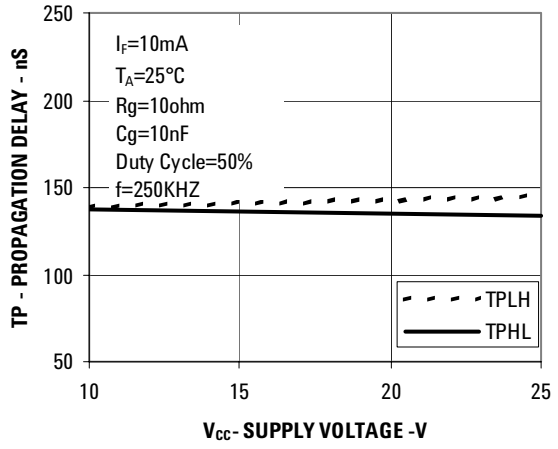


Figure 10. Propagation Delay Vs V_{CC}

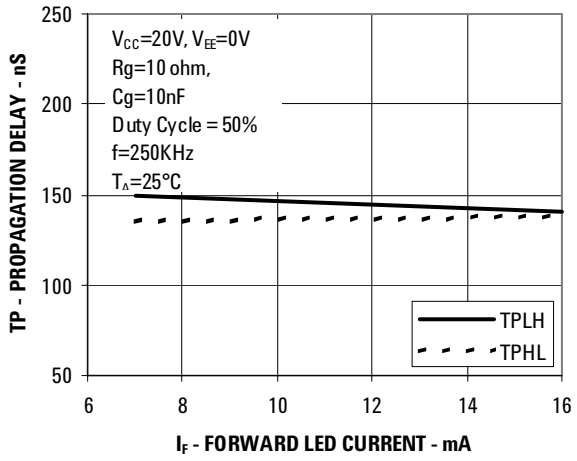


Figure 11. Propagation Delay Vs IF

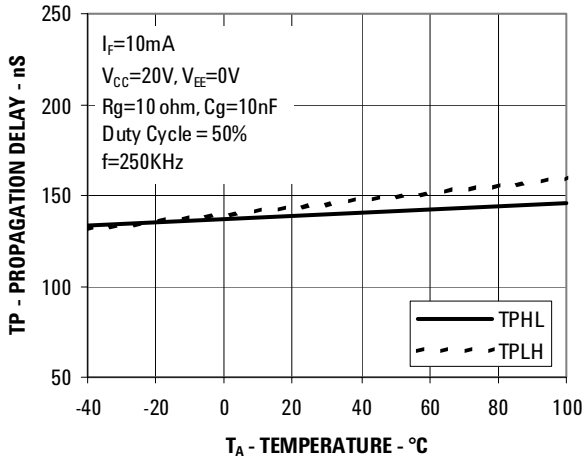


Figure 12. Propagation Delay Vs Temperature

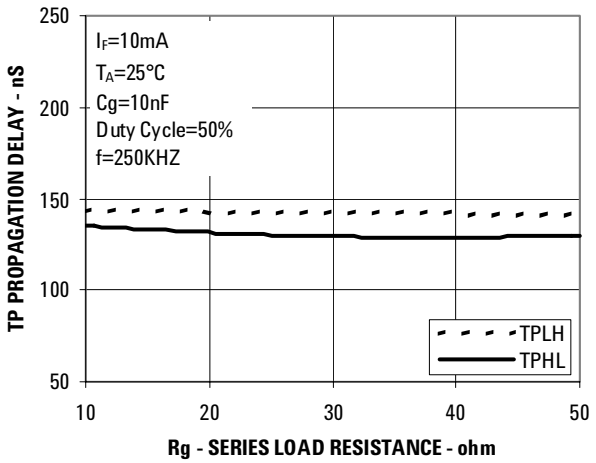


Figure 13. Propagation Delay Vs Rg

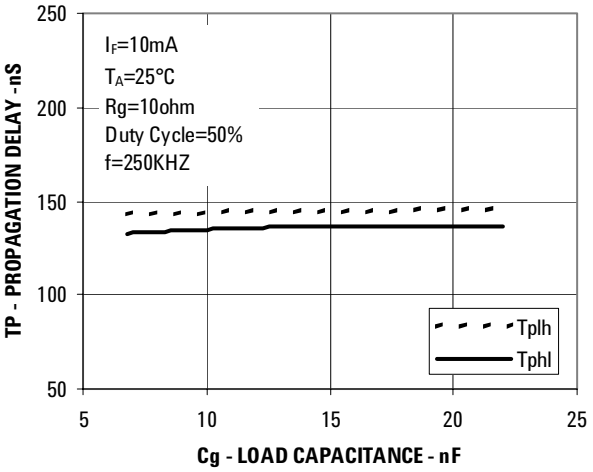


Figure 14. Propagation Delay Vs Cg

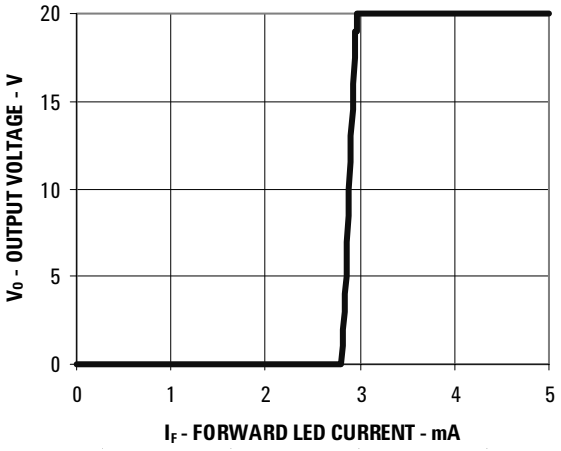


Figure 15. Transfer Characteristics

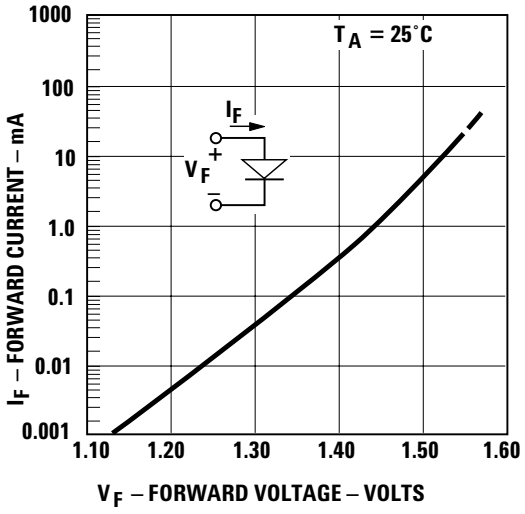


Figure 16. Input Current Vs Forward Voltage

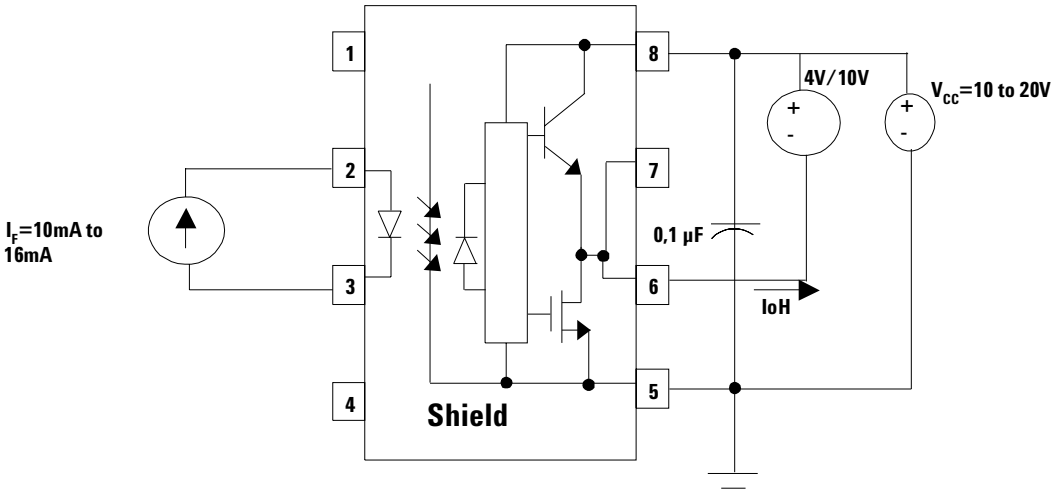


Figure 17. IOH Test Circuit

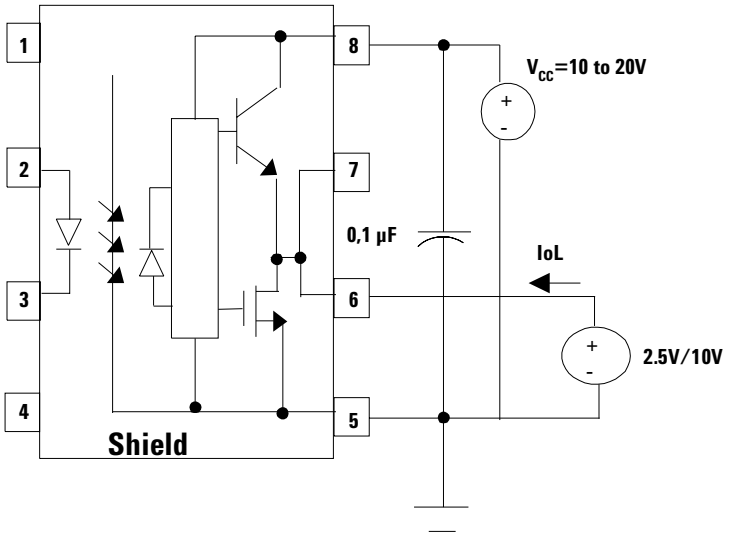


Figure 18. IOL Test Circuit

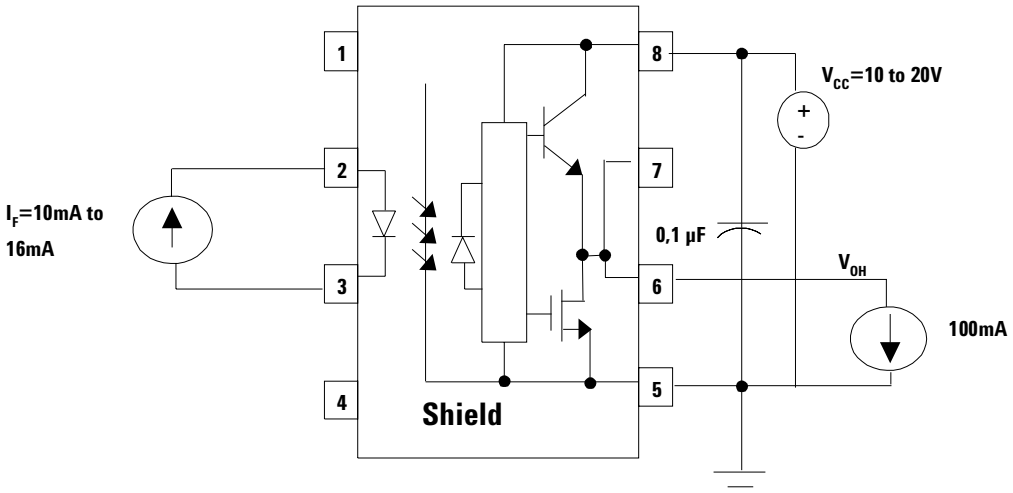


Figure 19. VOH Test Circuit

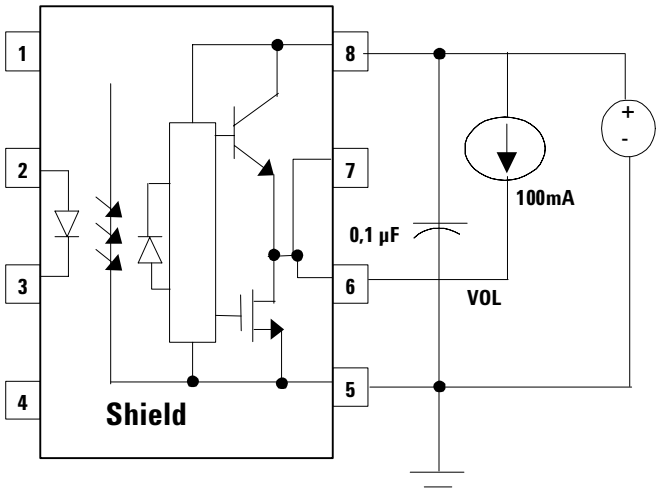


Figure 20. VOL Test Circuit

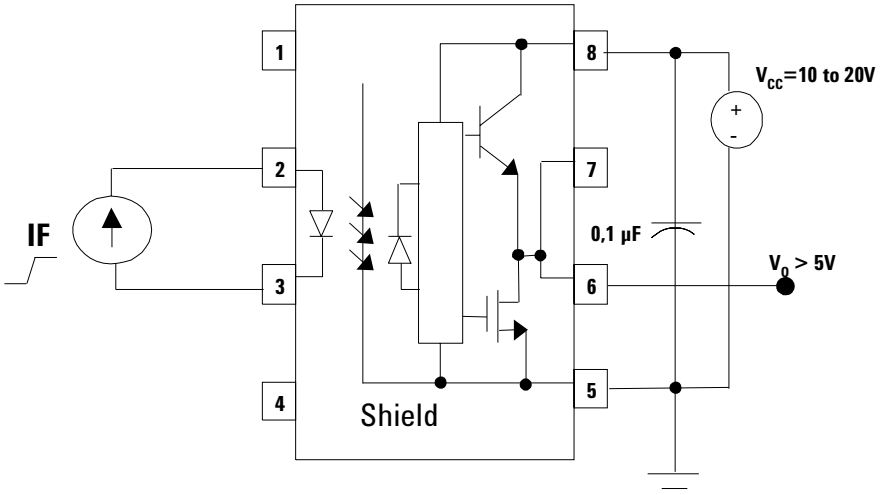


Figure 21. IFLH Test Circuit

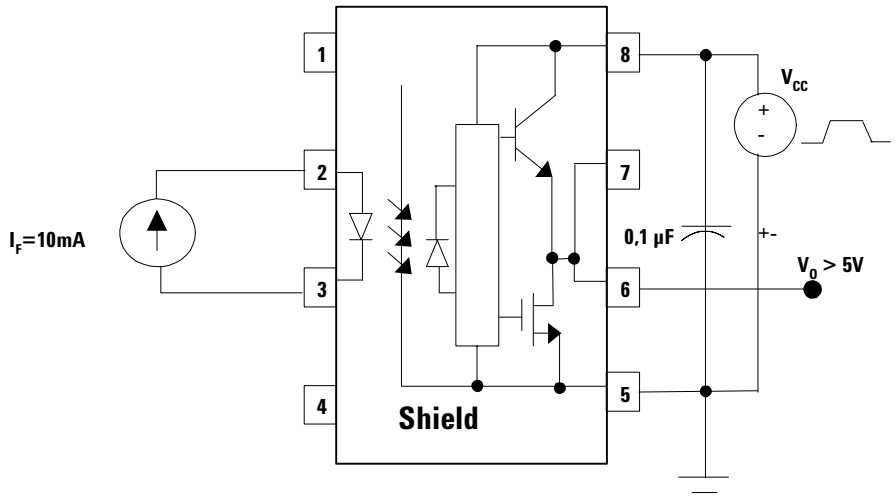


Figure 22. UVLO Test Circuit

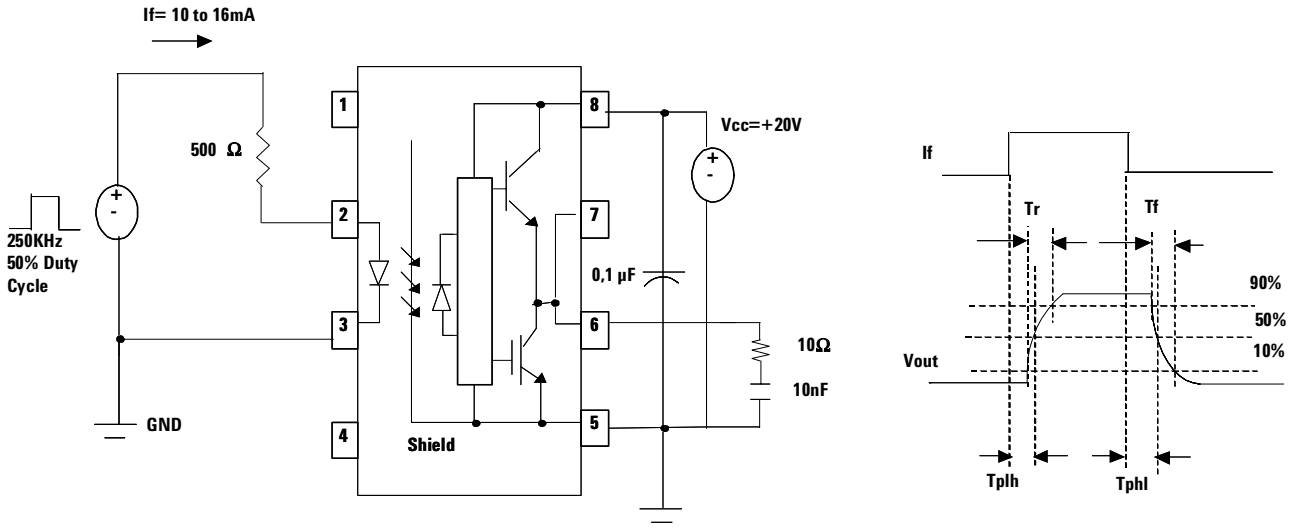


Figure 23. TPLH, TPHL, Tr and Tf Test Circuit and Waveform

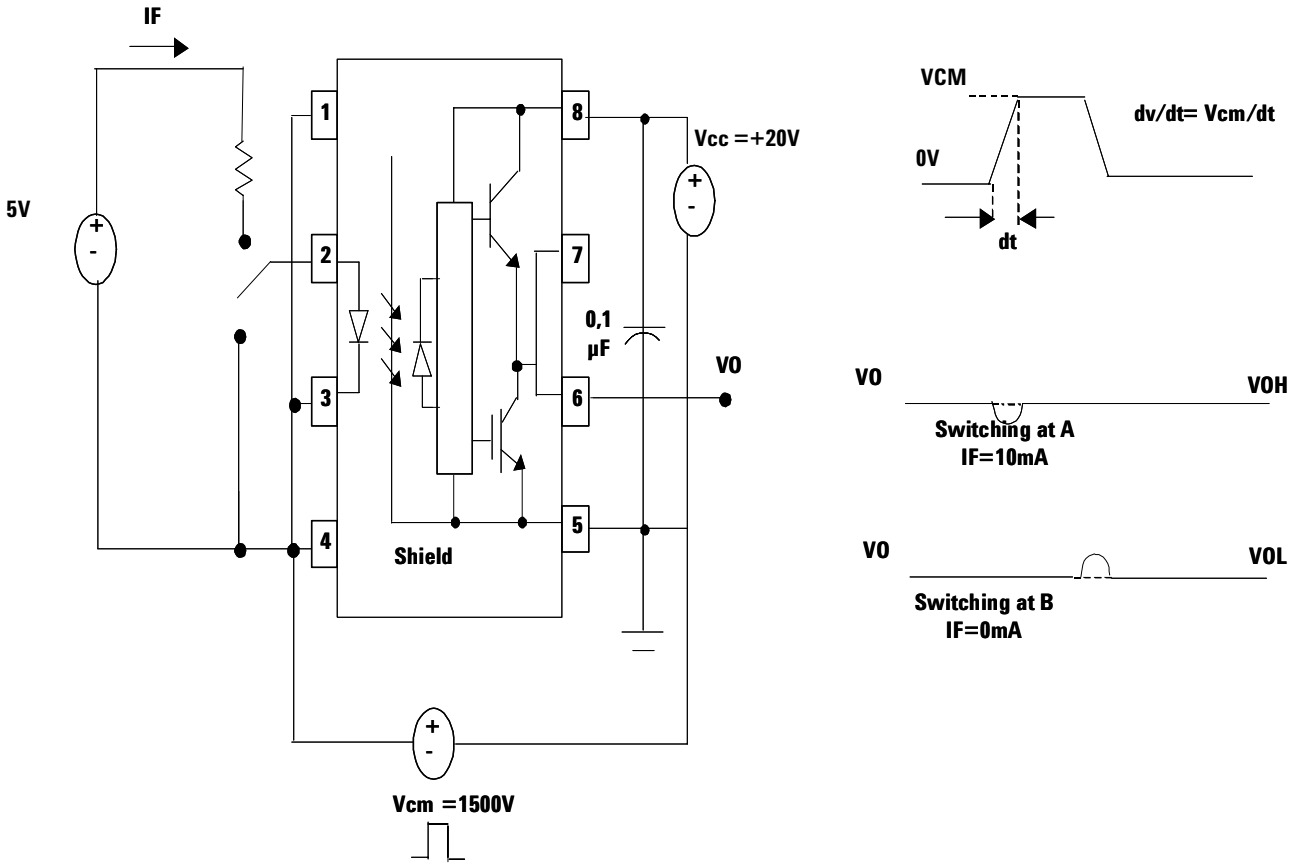


Figure 24. CMR Test Circuit and Waveform

Applications Information Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3180 has a very low maximum V_{OL} specification of 0.4 V. The HCPL-3180 realizes the very low V_{OL} by using a DMOS transistor with 1 W (typical) on resistance in its pull down circuit. When the HCPL-3180 is in the low state, the IGBT gate is shorted to the emitter by Rg + 1 W. Minimizing Rg and the lead inductance from the HCPL-3180 to the IGBT gate and emitter (possibly by mounting HCPL-3180 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3180 input as this can result in unwanted coupling of transient signals into the input of HCPL-3180 and degrade performance.

(If the IGBT drain must be routed near the HCPL-3180 input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3180)

Selecting the Gate Resistor (R_g) for HCPL-3180

Step 1: Calculate R_g minimum from the I_{OL} peak specification. The IGBT and R_g in Figure 25 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3180.

$$R_g \geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}} = \frac{20-3}{2} = 8.5\Omega$$

The V_{OL} value of 3 V in the previous equation is the V_{OL} at the peak current of 2 A. (See Figure 6).

Step 2: Check the HCPL-3180 power dissipation and increase R_g if necessary. The HCPL-3180 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$$P_T = P_E + P_O$$
$$P_E = I_F \bullet V_F \bullet \text{DutyCycle}$$
$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \bullet V_{CC} + E_{SW}(R_g; Q_g) \bullet f = (I_{CC}) \bullet V_{CC} + E_{SW}(R_g; Q_g) \bullet f$$

For the circuit in Figure 25 with the circuit in with I_F (worst case) = 16 mA, R_g ~ 10 W, Max Duty Cycle = 80%, Q_g = 100 nC, f = 200 kHz and T_{AMAX} = +75 °C:

$$P_E = 16mA \bullet 1.8V \bullet 0.8 = 23mW$$
$$P_O = 4.5mA \bullet 20V + 0.85\mu J \bullet 200kHz = 260mW \geq 226mW \begin{pmatrix} P_{O(MAX)} @ \\ 75°C \\ = 250mW \\ - (5°C * \\ 4.8mW / °C) \end{pmatrix}$$

The value of 4.5 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 6 mA to I_{CC} max at +75 °C. Since P_O for this case is greater than the $P_{O(max)}$, Rg must be increased to reduce the HCPL-3180 power dissipation.

$$P_o(SwitchingMAx) = P_0(Max) - P_O(Bias) = 226mW - 90mW = 136mW$$

$$E_{SW(Max)} = P_{O(Sitching\ Max)} / f = 136mW / 200KHz = 0.68\mu W$$

For Qg = 100 nC a Value of Esw = 0.68 UW gives a Rg = 15 ohm

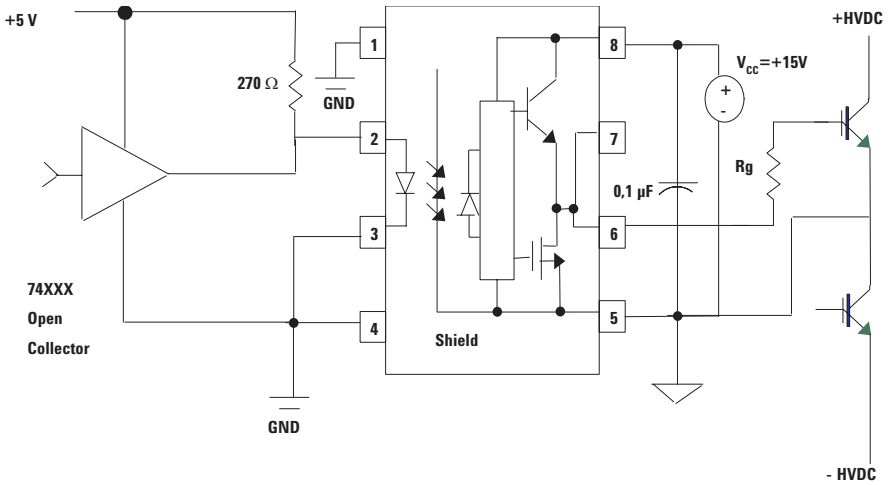


Figure 25. Recommended LED Drive and Application Circuit for HCPL-3180

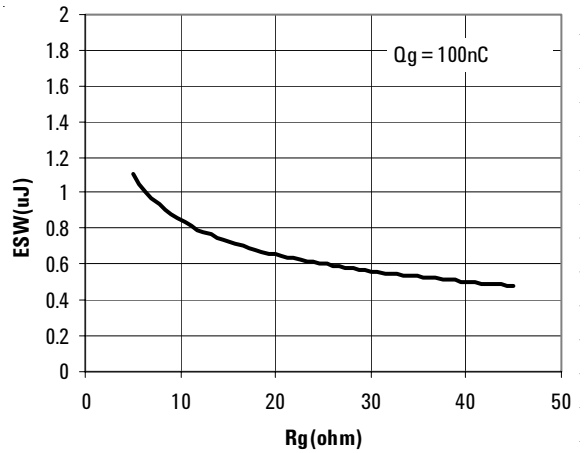


Figure 27. Energy Dissipated in the HCPL-3180 for each IGBT

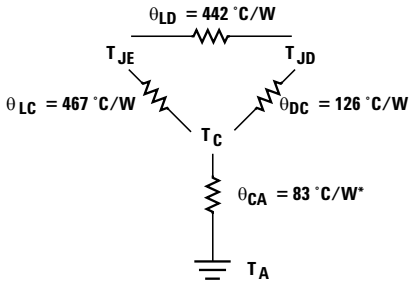


Figure 28. Thermal Model

Thermal Model
(Discussion applies to HCPL-3180)

The steady state thermal model for the HCPL-3180 is shown in Figure 28. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through Q_{CA} which raises the case temperature T_C accordingly. The value of Q_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of Q_{CA} = +83 °C/W was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single HCPL- 3180 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a Q_{CA} value of +83 °C/W From the thermal mode in Figure 28 the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E * (\theta_{LC} // (\theta_{LD} + \theta_{DC}) + \theta_{CA} + P_D * (\frac{\theta_{LC} * \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA}) + T_A$$

$$T_{JD} = P_E * (\frac{\theta_{LC} * \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA}) + P_D * (\theta_{DC} // (\theta_{LD} + \theta_{LC}) + \theta_{CA}) + T_A$$

Inserting the values for Q_{LC} and Q_{DC} shown in Figure 28 gives:

T_{JE} = PE·(+256 °C/W + Q_{CA})+ PD·(+57 °C/W + Q_{CA}) + T_A
T_{JD} = PE·(+57 °C/W + Q_{CA})+ PD·(+111 °C/W + Q_{CA}) + T_A

For example, given P_E = 45 mW,
P_O = 250 mW, T_A = +70 °C and QCA= +83 °C/W:
T_{JE} = PE·(+339 °C/W + PD·(+140 °C/W +T_A
= 45 mW·+339 °C/W + 250 mW·+140 °C/W + +70 °C
= +120 °C
T_{JD} = PE·(+140 °C/W + PD·+194 °C/W +T_A
= 45 mW·+140 °C/W + 250 mW·+194 °C/W + +70 °C
= +125 °C

T_{JE} and T_{JD} should be limited to +125 °C based on the board layout and part placement (QCA) specific to the application.

TJE = LED junction temperature
TJD = detector IC junction temperature
TC = case temperature measured at the center of the package bottom
Q_{LC} = LED-to-case thermal resistance
Q_{LD} = LED-to-detector thermal resistance
Q_{DC} = detector-to-case thermal resistance
Q_{CA} = case-to-ambient thermal resistance
*Q_{CA} will depend on the board design and the placement of the part.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 29. The HCPL-3180 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 30. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 10 kV/us CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

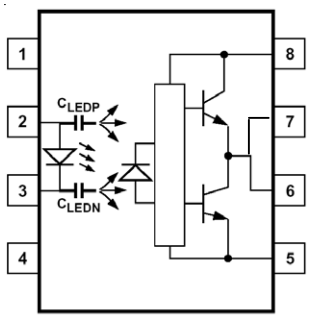


Figure 29. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

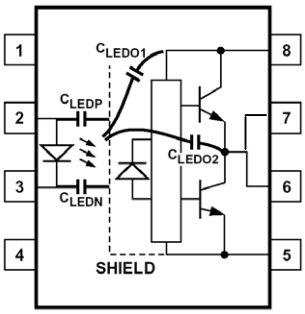


Figure 30. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

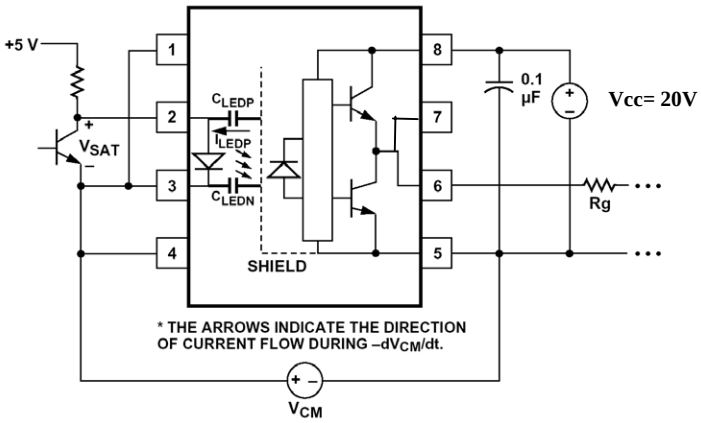


Figure 31. Equivalent Circuit for Figure 25 During Common Mode Transient.

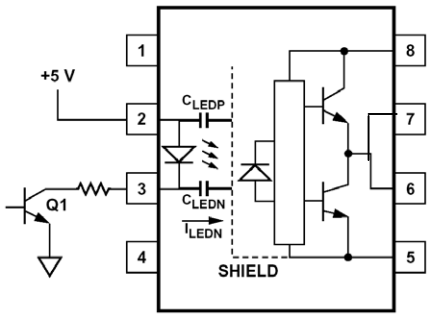


Figure 32. Not Recommended Open Collector Drive Circuit.

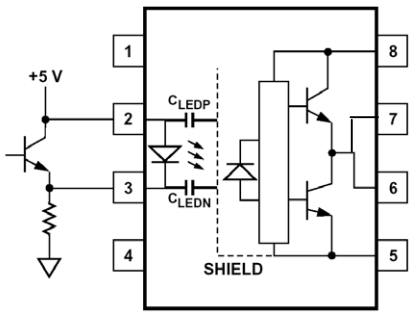


Figure 33. Recommended LED Drive Circuit for Ultra-High CMR

CMR with the LED On (CMR_H)
A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by over-driving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 8 mA to achieve 10 kV/us CMR.

CMR with the LED Off (CMR_L)
A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 31, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 32, cannot keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. Figure 33 is an alternative drive circuit, which like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

Under Voltage Lockout Feature
The HCPL-3180 contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the HCPL-3180 supply voltage (equivalent to the fully charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3180 output is in the high state and the supply voltage drops below the HCPL-3180 U_{VLO-} threshold (typ 7.5 V) the optocoupler output will go into the low state. When the HCPL-3180 output is in the low state and the supply voltage rises above the HCPL-3180 V_{UVLO+} threshold (typ 8.5 V) the optocoupler output will go into the high state (assume LED is "ON").

IPM Dead Time and Propagation Delay Specifications
The HCPL-3180 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power invertor designs. Dead time is the time during which the high and low side power transistors are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices from the high voltage to the low-voltage motor rails.

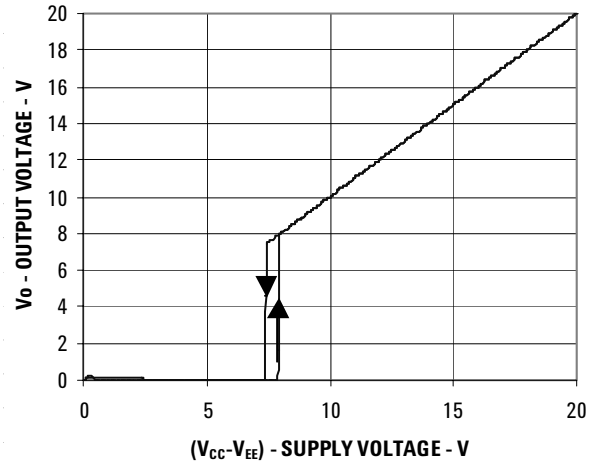
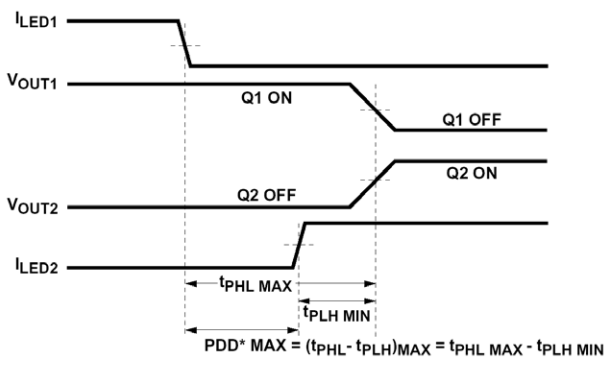


Figure 34. Under Voltage Lock Out



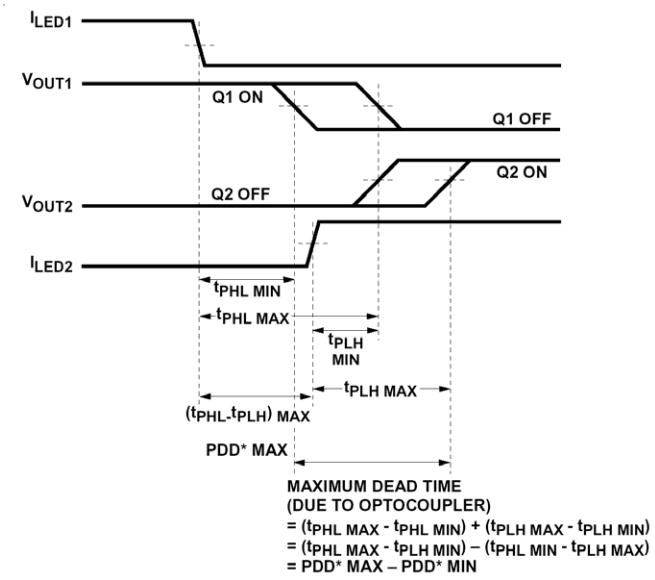
*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 35. Minimum LED Skew for Zero Dead Time

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 35. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 90 ns over the operating temperature range of -40 °C to +100 °C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 36. The maximum dead time for the HCPL-3180 is 180 ns (= 90 ns-(-90 ns)) over the operating temperature range of –40 °C to +100 °C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 36. Waveforms for Dead Time

www.agilent.com/
semiconductors

For product information and a complete list of distributors, please go to our web site.

For technical assistance call:
Americas/Canada: +1 (800) 235-0312 or
(916) 788-6763

Europe: +49 (0) 6441 92460

China: 10800 650 0017

Hong Kong: (+65) 6756 2394

India, Australia, New Zealand: (+65) 6755 1939

Japan: (+81 3) 3335-8152(Domestic/International), or
0120-61-1280(Domestic Only)

Korea: (+65) 6755 1989

Singapore, Malaysia, Vietnam, Thailand, Philippines,
Indonesia: (+65) 6755 2044

Taiwan: (+65) 6755 1843

Data subject to change.

August 11, 2003

5988-9921EN

Agilent Technologies