

1A, 600V N-CHANNEL MOSFET

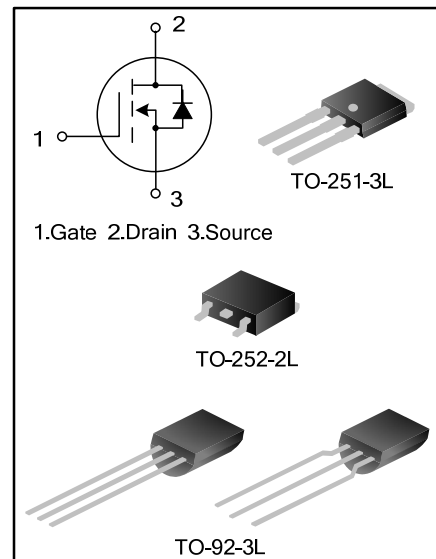
GENERAL DESCRIPTION

SVFM/B/D is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

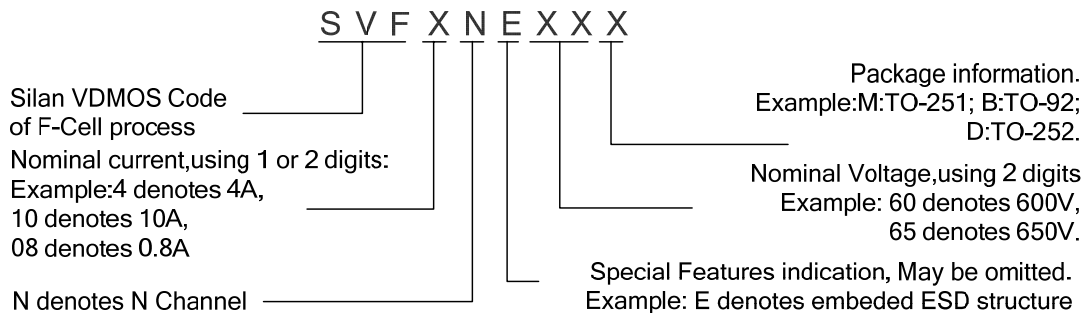
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- * 1A,600V, $R_{DS(on)}$ (typ.) =8.2Ω@ $V_{GS}=10V$
- * Low gate charge
- * Low Crss
- * Fast switching
- * Improved dv/dt capability



NOMENCLATURE



ORDERING SPECIFICATIONS

Part No.	Package	Marking	Material	Packing
SVF1N60M	TO-251-3L	SVF1N60M	Pb free	Tube
SVF1N60B	TO-92-3L	F1N60	Pb free	Bulk
SVF1N60BTR	TO-92-3L	F1N60	Pb free	AMMO
SVF1N60D	TO-252-2L	SVF1N60D	Pb free	Tube
SVF1N60DTR	TO-252-2L	SVF1N60D	Pb free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Rating		Unit
		SVF1N60B	SVF1N60M/D	
Drain-Source Voltage	V _{DS}	600		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current	I _D	T _C =25°C		A
		T _C =100°C		
Drain Current Pulsed	I _{DM}	4.0		A
Power Dissipation(T _C =25°C) -Derate above 25°C	P _D	9	28	W
		0.07	0.22	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	52		mJ
Operation Junction Temperature Range	T _J	-55~+150		°C
Storage Temperature Range	T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating		Unit
		SVF1N60B	SVF1N60M/D	
Thermal Resistance, Junction-to-Case	R _{θJC}	13.89	4.46	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	120	110	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B _{VDS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =0.5 A	--	8.2	11	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	--	140.15	--	pF
Output Capacitance	C _{oss}		--	19.43	--	
Reverse Transfer Capacitance	C _{rss}		--	18.95	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =1.0A, R _G =25Ω (Note 2,3)	--	6.47	--	ns
Turn-on Rise Time	t _r		--	13.27	--	
Turn-off Delay Time	t _{d(off)}		--	7.73	--	
Turn-off Fall Time	t _f		--	15.87	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =1.0A, V _{GS} =10V (Note 2,3)	--	3.45	--	nC
Gate-Source Charge	Q _{gs}		--	1.10	--	
Gate-Drain Charge	Q _{gd}		--	1.39	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_s	Integral Reverse P-N Junction Diode in the MOSFET	--	--	1.0	A
Pulsed Source Current	I_{SM}		--	--	4.0	
Diode Forward Voltage	V_{SD}	$I_s=1.0A, V_{GS}=0V$	--	--	1.5	V
Reverse Recovery Time	T_{rr}	$I_s=1.0A, V_{GS}=0V,$ $dI_F/dt=100A/\mu S$ (Note 2)	--	190	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.53	--	μC

Notes:

1. $L=30mH, I_{AS}=1.74A, V_{DD}=85V, R_G=25\Omega,$ starting $T_J=25^\circ C;$
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%;$
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

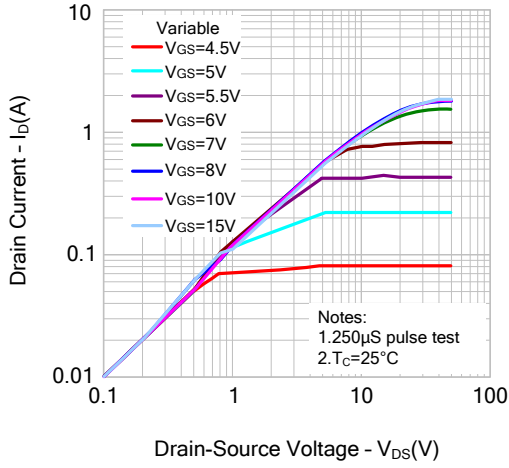


Figure 2. Transfer Characteristics

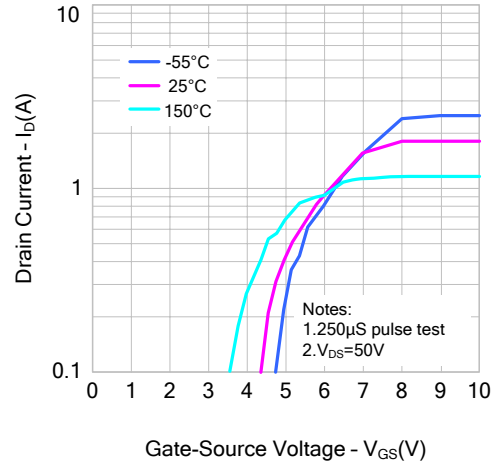


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

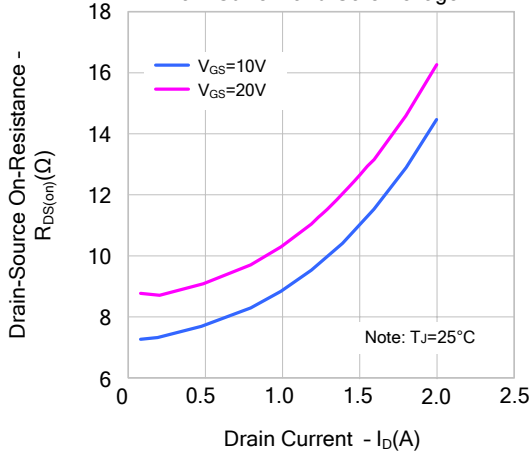


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

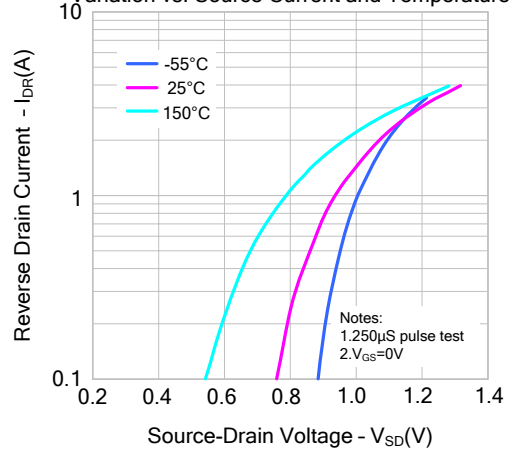


Figure 5. Capacitance Characteristics

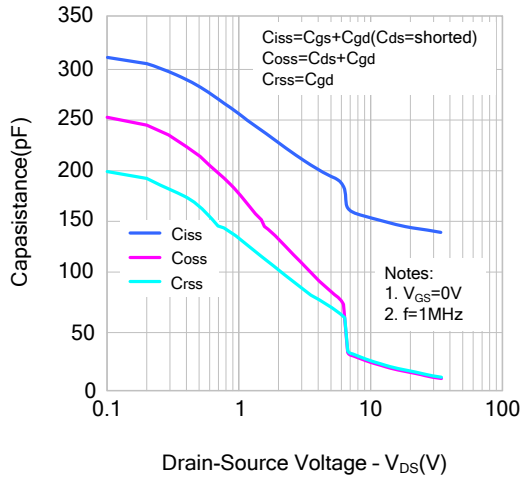
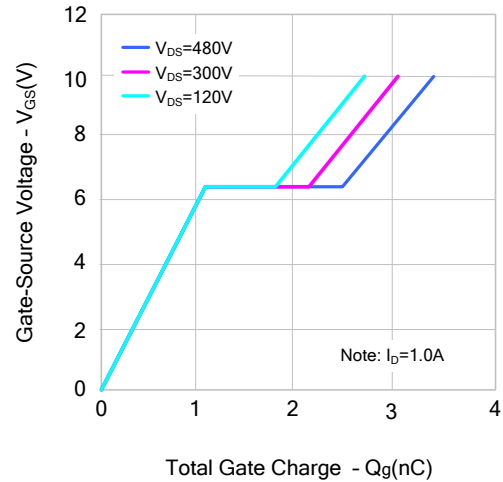


Figure 6. Gate Charge Characteristics





TYPICAL CHARACTERISTICS (continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

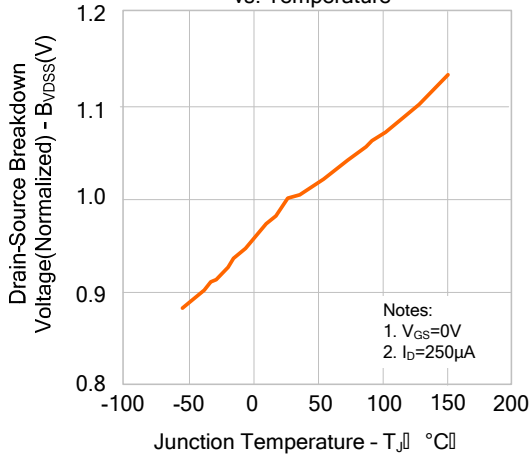


Figure 8. On-resistance Variation vs. Temperature

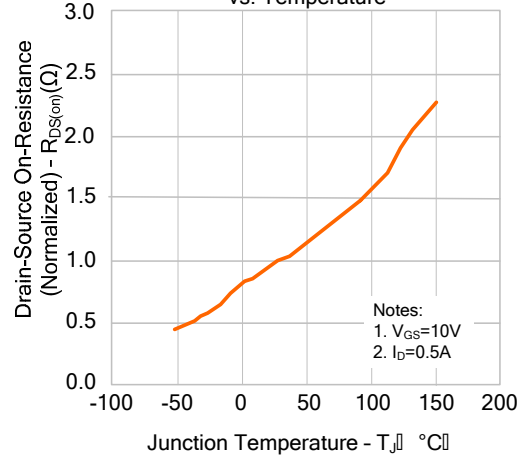


Figure 9-1. Max. Safe Operating Area(SVF1N60B)

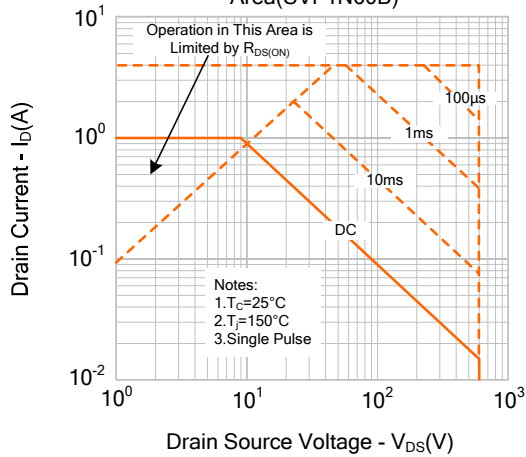


Figure 9-2. Max. Safe Operating Area(SVF1N60M/D)

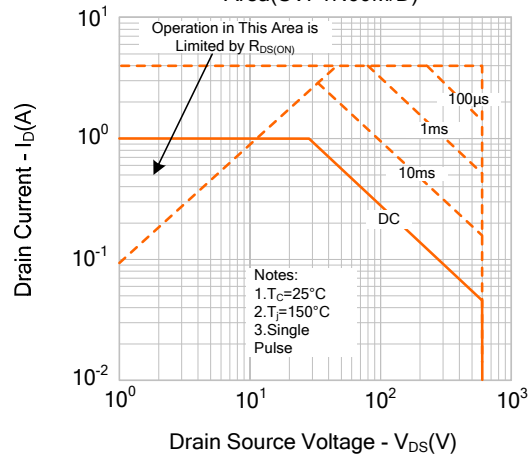
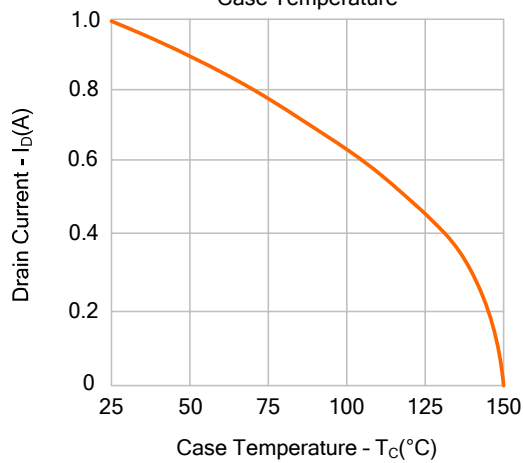
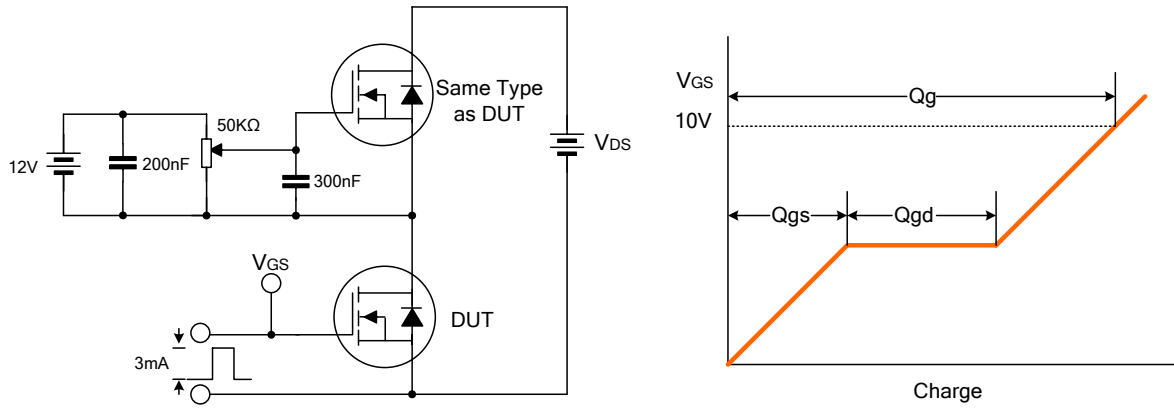


Figure 10. Maximum Drain Current vs. Case Temperature

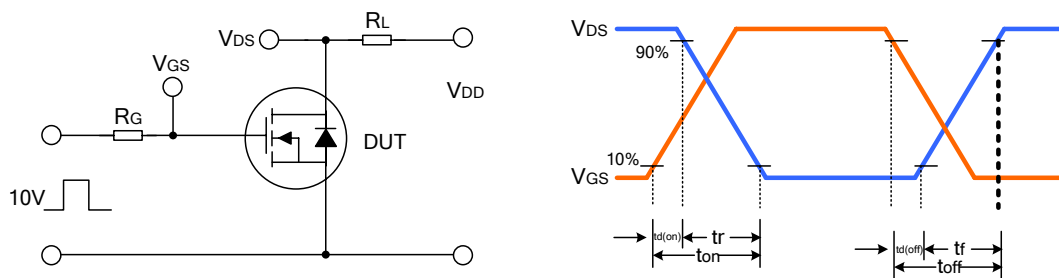


TYPICAL TEST CIRCUIT

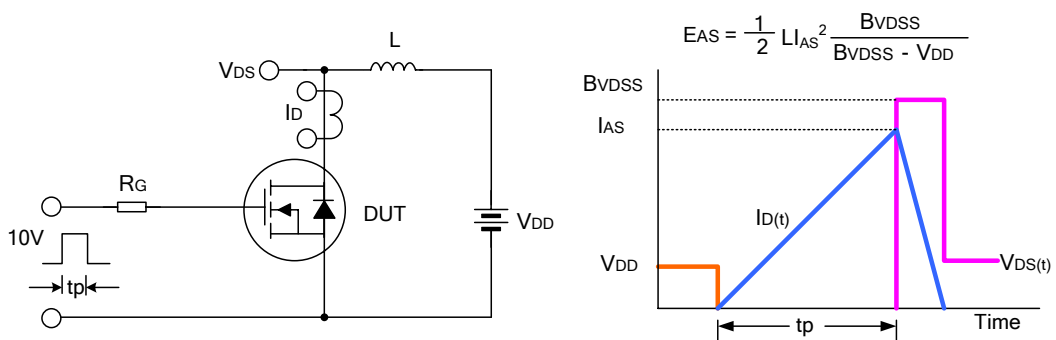
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



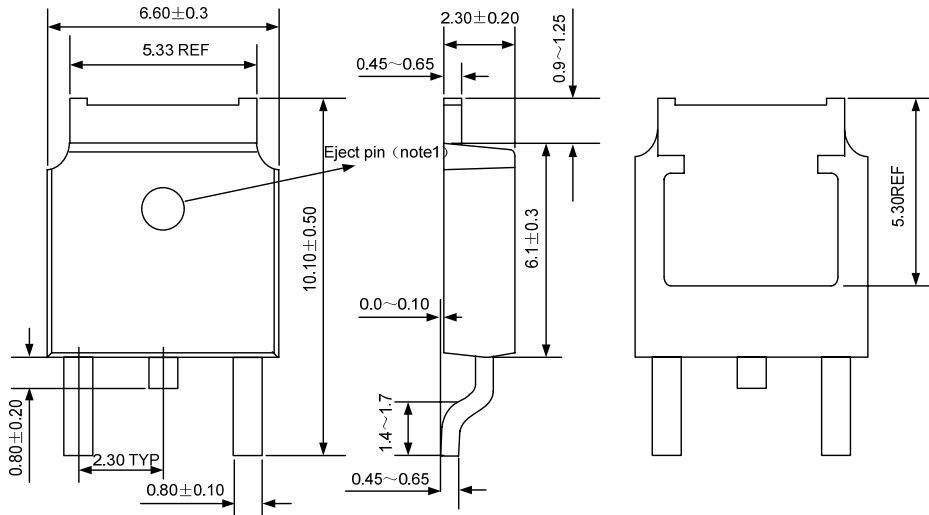
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

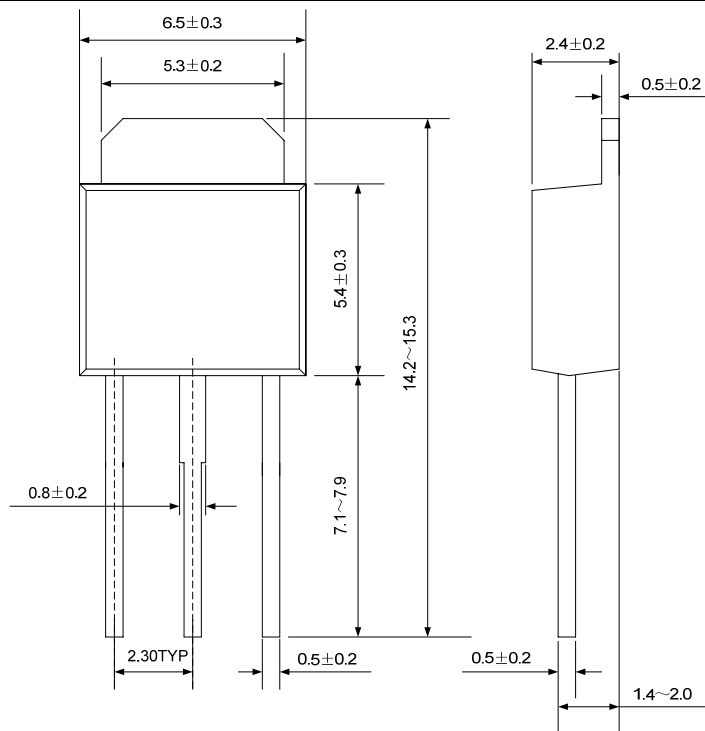
UNIT: mm



NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-251-3L

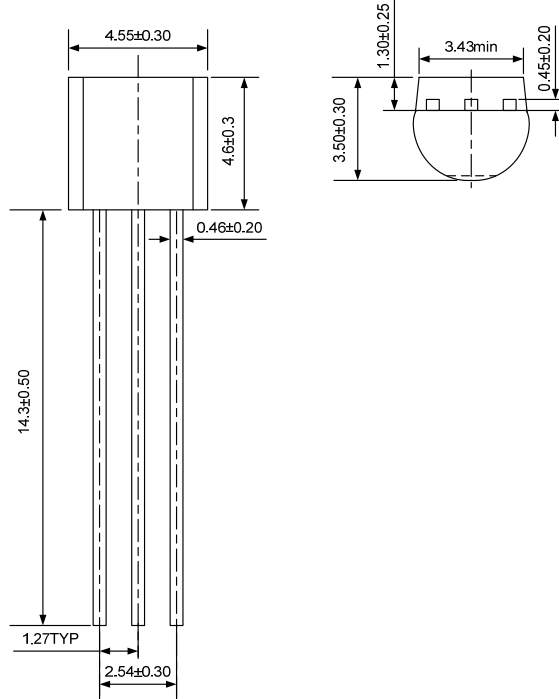
UNIT: mm



PACKAGE OUTLINE (continued)

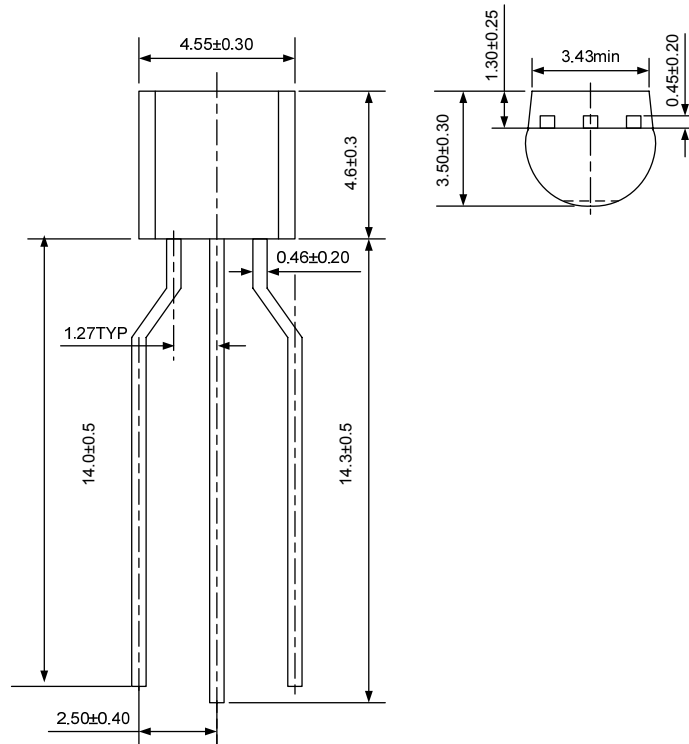
TO-92-3L(One)

UNIT: mm



TO-92-3L(Two)

UNIT: mm





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- Silan will supply the best possible product for customers!

ATTACHMENT

Revision History

Date	REV	Description	Page
2011.03.30	1.0	Original	