Application Note	*THAN0064_Rev1.40_E*

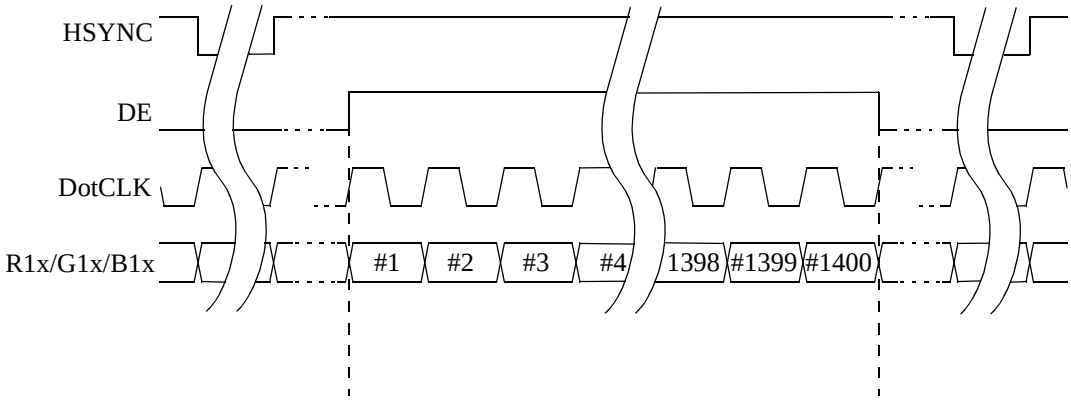
THC63LVD103(D)/THC63LVD105/THC63LVD104S(C) ApplicationNote

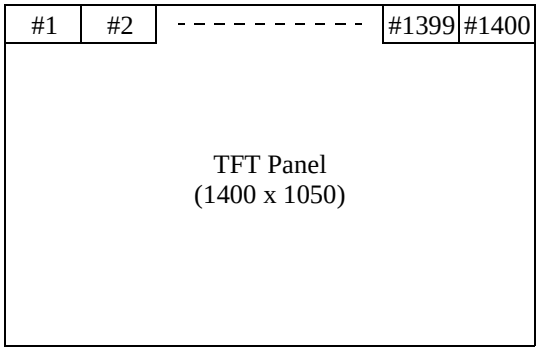
System Diagram and PCB Design Guide Line

Contents

1. TTL DATA Timing Diagram

Following are THC63LVD103(D)/THC63LVD105 TTL data input timing example for SXGA+(1400 x 1050).

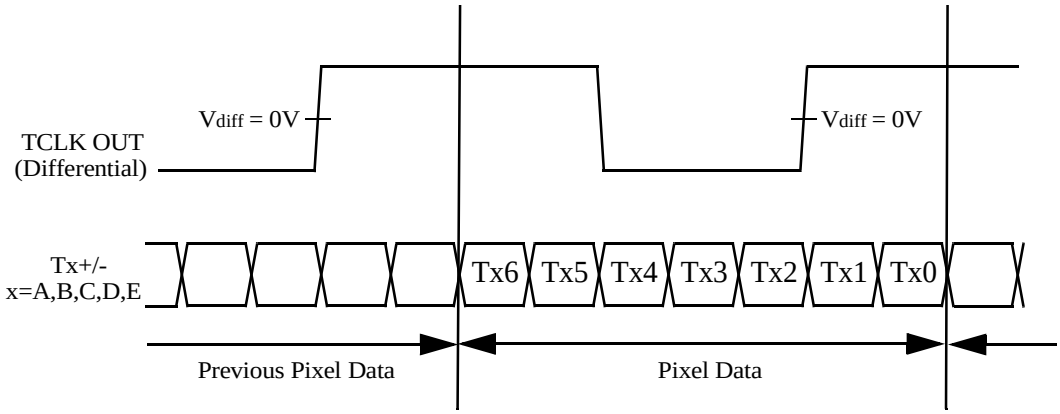




Note:

	Red	Green	Blue
MSB	R9	G9	B9
	R8	G8	B8
	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
6bit LSB	R4	G4	B4
	R3	G3	B3
8bit LSB	R2	G2	B2
	R1	G1	B1
10bit LSB	R0	G0	B0

2.LVDS DATA Timing Diagram



THC63LVD103(D)/THC63LVD105/THC63LVD104S(C) Pixel Data Assign (6bit,8bit,10bit Application)

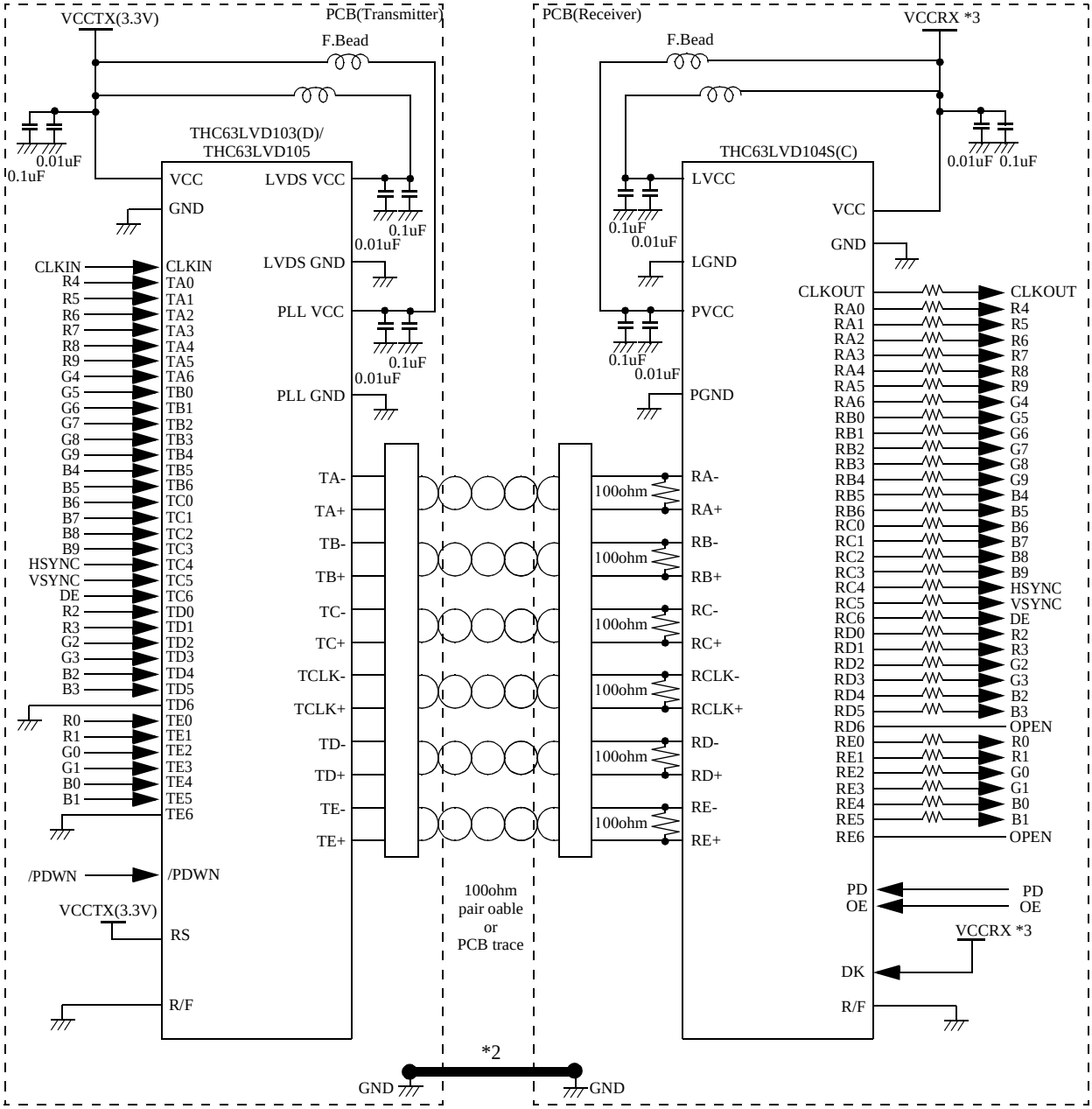
	6bit	8bit	10bit
TA0	R4	R4	R4
TA1	R5	R5	R5
TA2	R6	R6	R6
TA3	R7	R7	R7
TA4	R8	R8	R8
TA5	R9	R9	R9
TA6	G4	G4	G4
TB0	G5	G5	G5
TB1	G6	G6	G6
TB2	G7	G7	G7
TB3	G8	G8	G8
TB4	G9	G9	G9
TB5	B4	B4	B4
TB6	B5	B5	B5
TC0	B6	B6	B6
TC1	B7	B7	B7
TC2	B8	B8	B8
TC3	B9	B9	B9
TC4	Hsync	Hsync	Hsync
TC5	Vsync	Vsync	Vsync
TC6	DE	DE	DE
TD0	-	R2	R2
TD1	-	R3	R3
TD2	-	G2	G2
TD3	-	G3	G3
TD4	-	B2	B2
TD5	-	B3	B3
TD6	-	N/A	N/A
TE0	-	-	R0
TE1	-	-	R1
TE2	-	-	G0
TE3	-	-	G1
TE4	-	-	B0
TE5	-	-	B1
TE6	-	-	N/A

Note:For 6bit application,use A~C channel and open TD+/-,TE+/- pin.
:For 8bit application,use A~D channel and open TE+/- pin.

3. Example of System Diagram

1)10 bit TTL/CMOS Input

Example:
THC63LVD103(D)/THC63LVD105 :FAlling edge/Normal swing
THC63LVD104S(C) :Falling edge



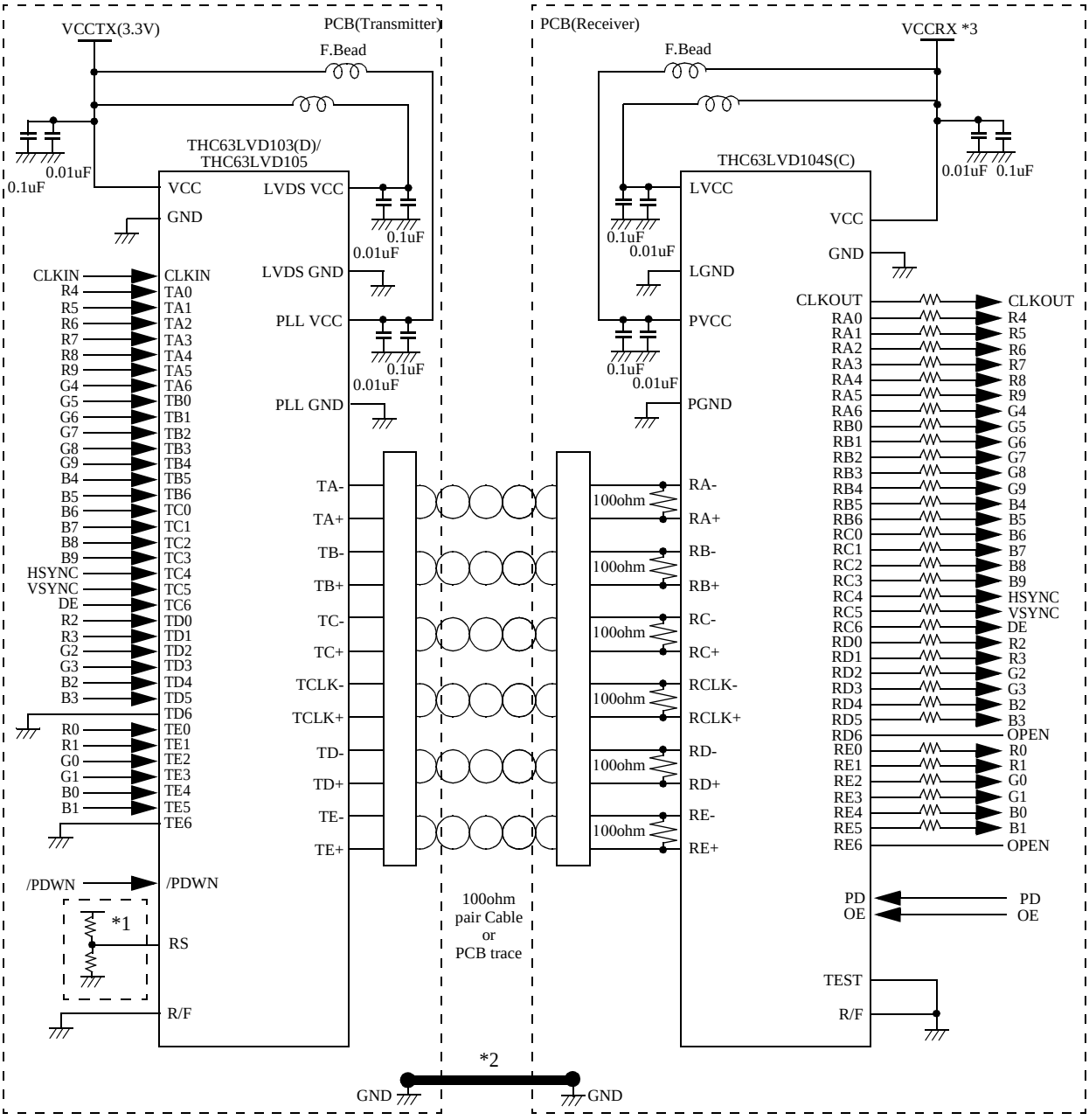
*1:If RS pin is tied to VCCTX, LVDS swing is 350mV.
If RS pin is tied to GND, LVDS swing is 200mV.

*2:Connect each PCB GND

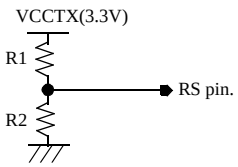
*3: THC63LVD104S = 2.5V
THC63LVD104C = 3.3V

2)10 bit Small Swing Level Input

Example:
THC63LVD103(D)/THC63LVD105 :FAlling edge/Normal swing
THC63LVD104S(C) :Falling edge



*1:RS pin acts as VREF input pin when input voltage is set to half of high level signal input.



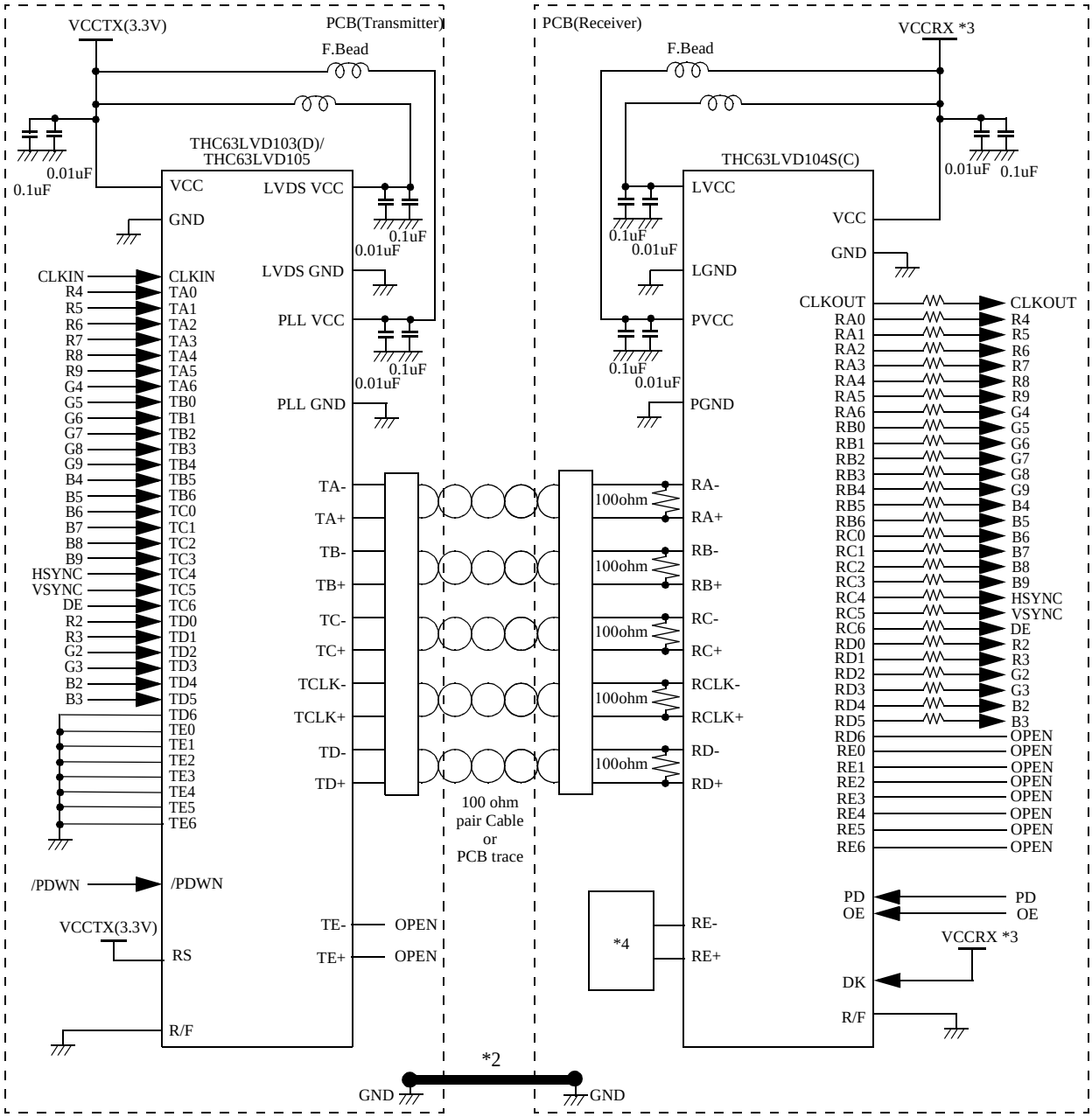
Example for Small Swing input (R1,R2)=(3.3kohm,1kohm~2.2kohm)

*2:Connect each PCB GND

*3: THC63LVD104S = 2.5V
THC63LVD104C = 3.3V

3)8 bit TTL/CMOS Level Input

Example:
THC63LVD103(D)/THC63LVD105 :Small Swing input/Falling edge/Small swing
THC63LVD104S(C) :Falling edge

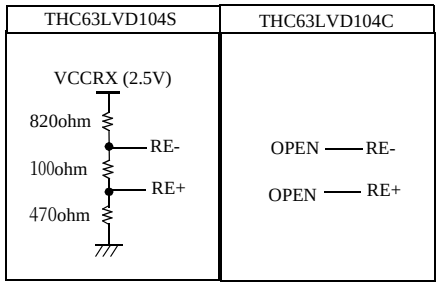


*1:If RS pin is tied to VCCTX, LVDS swing is 350mV.
If RS pin is tied to GND, LVDS swing is 200mV.

*2:Connect each PCB GND

*3: THC63LVD104S = 2.5V
THC63LVD104C = 3.3V

*4



4. Note

1)Output Control

THC63LVD103(D)/THC63LVD105

/PDWN	Input(TTL)	Output(LVDS)
L	Open or Hi-z	Hi-z
L	Input CLK	Hi-z
H	Open or Hi-z	Hi-z
H	Input CLK *1	Data, CLK Out

THC63LVD104S(C)

PD	OE	Input(LVDS)	Output(TTL)
L	L	Open or Hi-z	Hi-z
L	L	Input CLK	Hi-z
L	H	Open or Hi-z	All Low
L	H	Input CLK	All Low
H	L	Open or Hi-z	Hi-z
H	L	Input CLK	Hi-z
H	H	Open or Hi-z	All Low
H	H	Input CLK *1	Data, CLK Out

*1 With in the range of Recommended Operating Conditions. Refer to Recommended Operating Conditions on data sheet. Without the range, each Output(TTL) signal is unfixed Data, CLK Out.

2)Power On Sequence

Power on THC63LVD103(D)/THC63LVD105 after THC63LVD104S(C). If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

3)Cable Connection and Disconnection

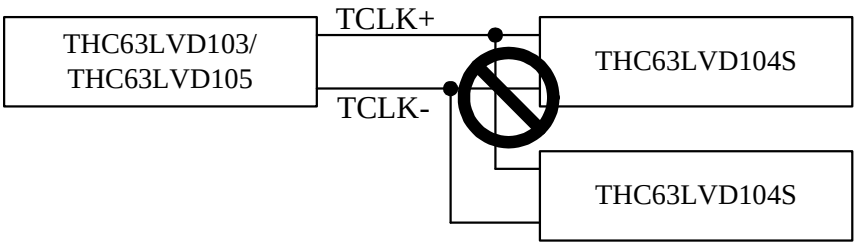
Don’t connect and disconnect the LVDS cable , when the power is supplied to the system.

4)GND Connection

Connect the each GND of the PCB which THC63LVD103(D)/THC63LVD105 and THC63LVD104S(C) on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

5)Multi Drop Connection

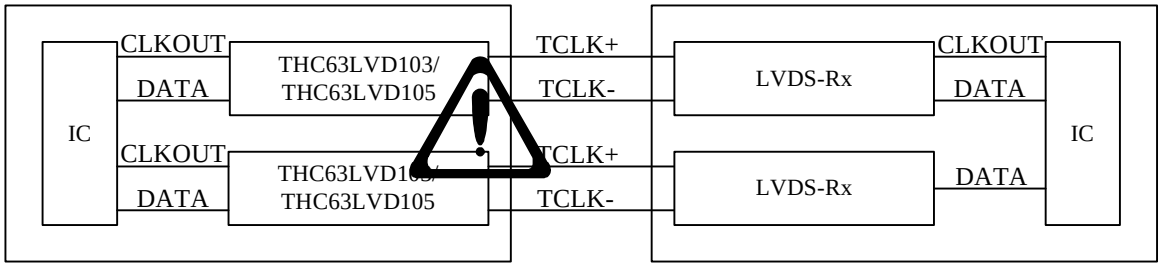
Multi drop connection is not recommended.

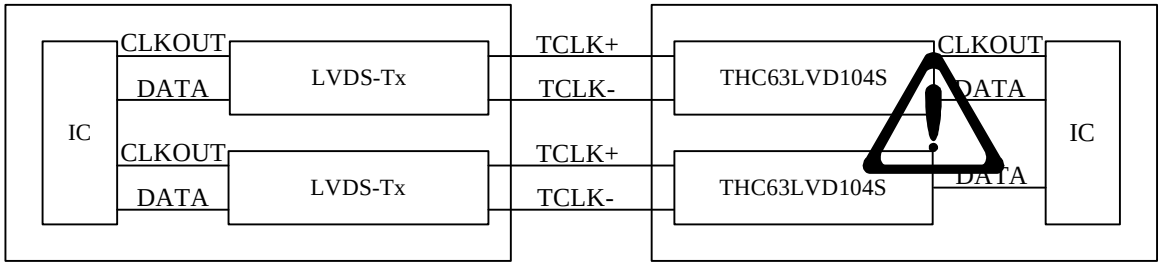


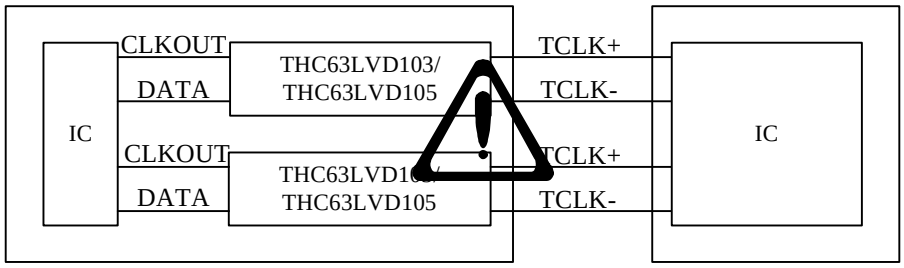
6)Asynchronous use

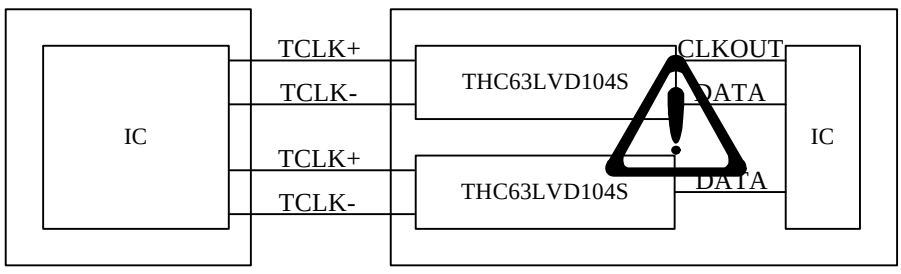
Asynchronous use such as following systems are not recommended. If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)









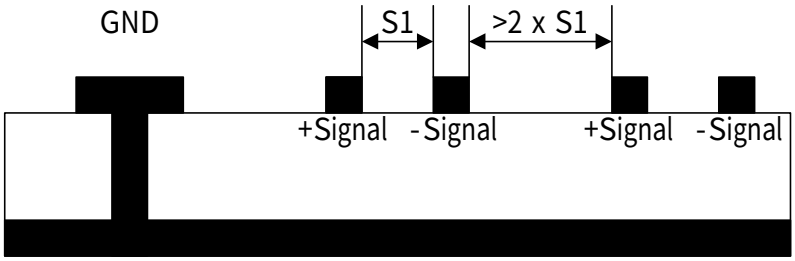
5. PCB Design Guide Line

General Guideline

- Use 4 layer PCB (minimum).
- Locate by-pass capacitors adjacent to the device pins as close as possible.
- Make the loop minimum which is consist of Power line and Gnd line.

LVDS Traces

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as much as possible.
- Avoid 90 degree bends.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place Terminal Resister adjacent to the Receiver.



Attentions and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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